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Indium Phosphide Planar Gunn Diode

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ADMINISTRATIVE INFORMATION

This work was performed for the Office of the Chief of Naval Research, Independent Research Programs (IR), Arlington, VA 22217-5000, under program element 0601152N. This work was performed by members of NOSC Codes 561 and 753.

The experiments involving InP Gunn diodes covered by this report were completed in December 1987. Due to lack of funds, the results were not published until later.

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INTRODUCTION

Monolithic microwave circuits normally require such extensive processing that the fabrication of less than several thousand identical circuits is rarely considered. At millimeter-wave frequencies the required precision generally increases and additional steps, including electron beam lithography (for transistor gate definition) and ion implantation (for contact definition), are often required.

It was our intent to develop indium phosphide (InP) monolithic circuits using truly planar Gunn diodes as active devices. Processing would only involve epitaxial growth (metalorganic chemical vapor deposition [MOCVD] or vapor phase epitaxy [VPE]), photolithography involving dimensions of 3 μm or more, and the various processes used at lower frequencies. To test the devices in hybrid circuits, gold foil beam leads would also be fabricated.

At the end of our 2-year program, beam-leaded devices oscillated on hybrid circuits in the 20- to 40-GHz range. Pulsed output power was about 4 mW. Pulsing was required because heat sinking was not used.

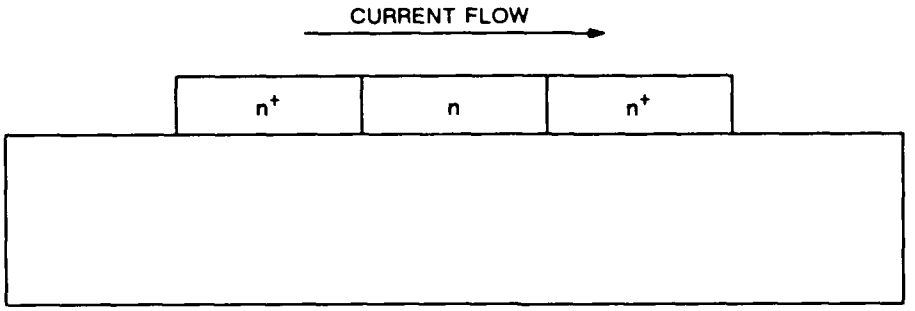
This report covers work completed in December 1987.

BACKGROUND

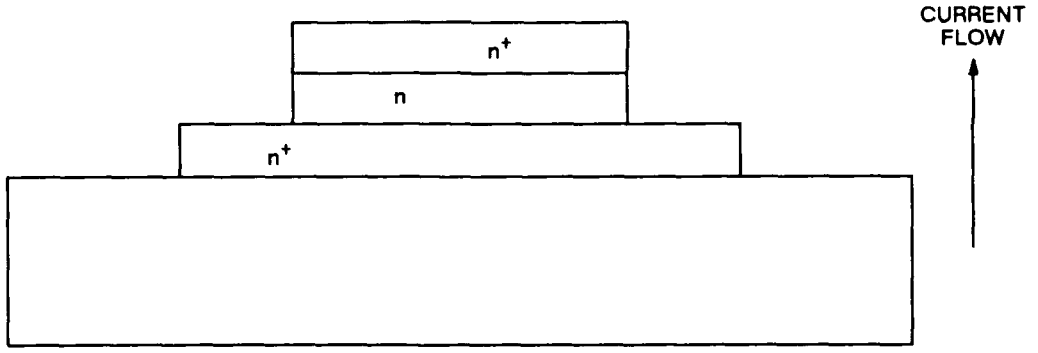
Although InP is the material of choice for efficient millimeter-wave Gunn-effect diodes, all monolithic oscillators built to date have used GaAs. These devices have been fabricated in mesa form, where current flows in a direction perpendicular to the substrate. To bring the lower terminal to the top of the substrate, ion implantation is used to create a conductive channel surrounding the mesa. The planar Gunn diode (figure 1), unlike the mesa Gunn diode, has its current flowing parallel to the surface. Contacts can be made directly to the two ends of the diode. In the early 1970s the planar Gunn diode was used in the 10-GHz-frequency range by several companies, including RCA. Similar devices have never been reported to operate at millimeter-wave frequencies.

Binari, Thompson, and Grubin (1985) of the Naval Research Laboratory have developed an ion-implanted planar InP Gunn diode. However, this diode operated only when additional ion implant damage (oxygen implant) was used to define a narrow region near the cathode where the domains are initiated. Another planar Gunn device, developed in Austria, uses a third terminal for control (Hartwig, February 1987).

During the initial phase of this project, scanning electron microscope (SEM) photos indicated that etching the epitaxial material to produce the active Gunn region generally resulted in sloped walls of 40 degrees or more. This was true unless the diode was oriented along one particular crystallographic direction. The Gunn effect is transit-time dependent, and at 30 GHz, sloped walls could result in as much as a 25-percent difference in transit times between current traveling along the top and along the bottom of the 0.5- to 1.0-μm-thick device. This difference in geometry was carefully monitored and utilized during all subsequent processing.



(a) PLANAR GUNN DEVICE



(b) MESA GUNN DEVICE

Figure 1. (a) Planar Gunn diode showing current flow parallel to the wafer surface, (b) mesa Gunn diode showing current flow perpendicular to the wafer surface.

EXPERIMENTAL APPROACH

EPITAXIAL LAYER GROWTH

The surface-oriented planar Gunn diode was fabricated from epitaxial layers sequentially grown as outlined in figure 2. Starting with a piece of semi-insulating iron-doped InP, an epitaxial layer of nominally undoped InP (carrier concentration $\approx 10^{16}$ cm^{-3}) was grown by MOCVD on the polished (100) surface. After selectively removing portions of the first epitaxial layer, a second epitaxial layer of higher carrier concentration ($n \approx 10^{18}$ cm^{-3}) was grown in the recesses, creating the structure of figure 2c.

The epitaxial layers used in this program were primarily grown by MOCVD in an in-house reactor, using trimethylindium and phosphine as source materials for the epilayer and silane as the dopant source. Additional layers were provided by Varian Associates, using a VPE growth system, solid indium and phosphorus trichloride as source materials for the epilayer, and hydrogen sulfide as the dopant source.

The epitaxially grown planar Gunn diode had two unique requirements. First, since the second epilayer was to be grown in selected areas only, a masking layer was needed. This layer had to be stable at the InP growth temperatures ($\approx$ 650°C), not provide nucleation sites for InP formation, and be easily removed for subsequent wafer processing. Second, because of the transit-time dependence on geometry as noted earlier, vertical walls of the recess profile were needed to insure a single transit length. These two issues were investigated in detail by Taylor and Schumacher (March 1988).

After considerable experimentation, silicon dioxide (SiO_2) was chosen as the masking layer for selectively etching the first epilayer and regrowing the second layer. The chemical etchant used to produce vertical sidewalls in the first epilayer was $HCl:H_3PO_4$ 1:9. This resulted in vertical walls parallel to the $\langle 011 \rangle$ direction and sloped walls parallel to the $\langle 0\bar{1}1 \rangle$ direction. Most diode structures were oriented so the transit path of the current would be in the $\langle 0\bar{1}1 \rangle$ direction (vertical interface between n and n^+ regions). For comparison, some diodes were oriented 90 degrees from this (with the n/n^+ interface a sloped profile).

The epilayer growth/regrowth process encountered several unexpected problems. Not only was the wall profile of the interface dependent on crystal orientation (easily addressed by device orientation), but the bulk InP on which the epilayers were grown came from different suppliers, and materials from each supplier etched quite differently. Representative photos of etch tests are shown in figure 3. Some of the differences in surface features can be attributed to the following : (a) quality of the starting crystal, i.e., purity of the material, degree of contamination, number of inclusions, etc., (b) surface finish and degree of subsurface damage still remaining. Material quality is a continuing concern for InP users. Suppliers are constantly seeking to improve the bulk quality and surface finish of InP wafers. Each year improvements are made in these areas.

Substrate surface treatment also had a significant effect on the surface morphology of the subsequent epilayer. Unavoidable surface treatment included

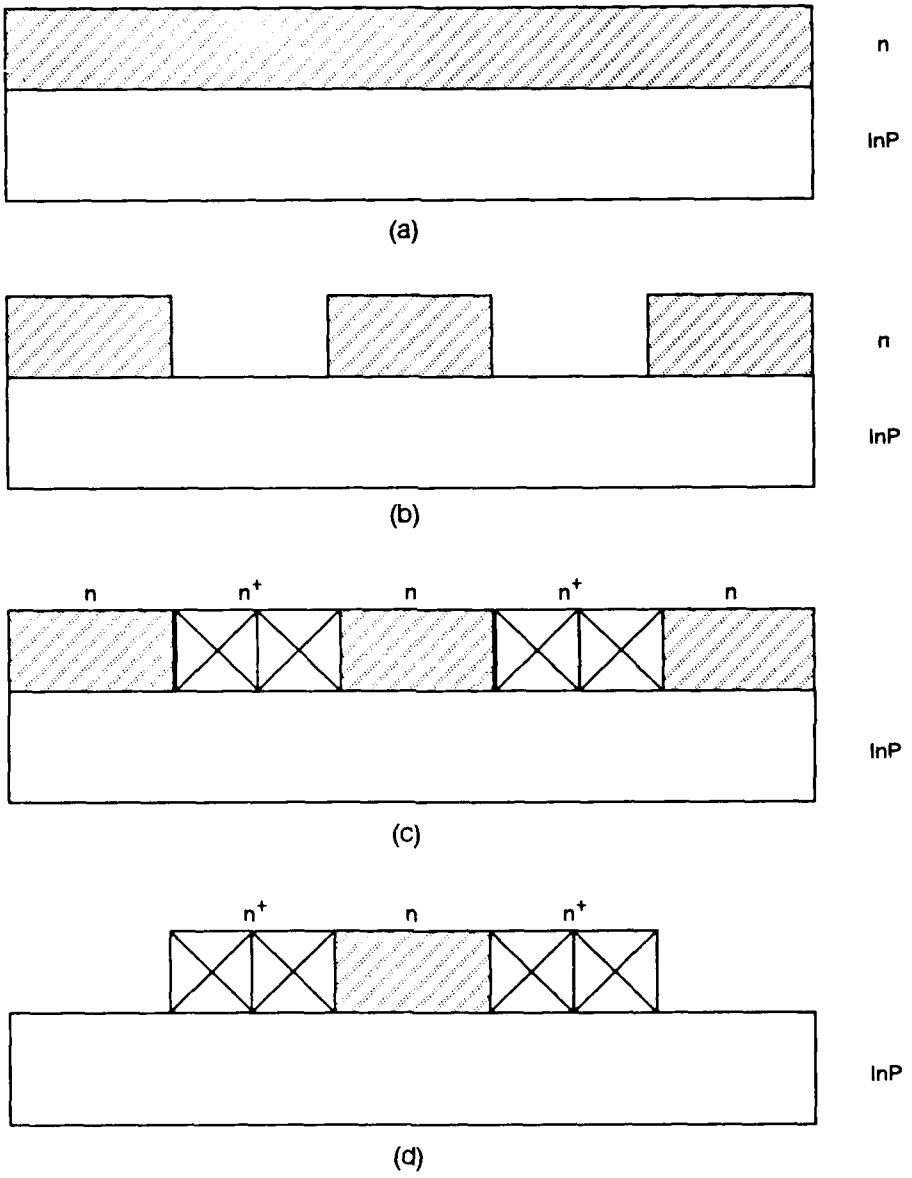
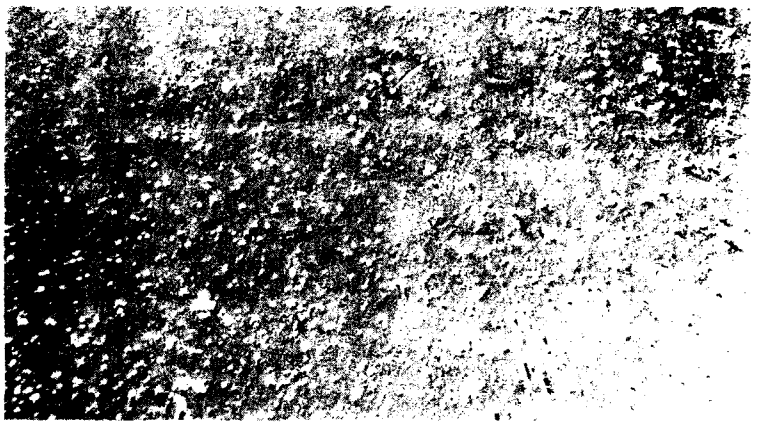
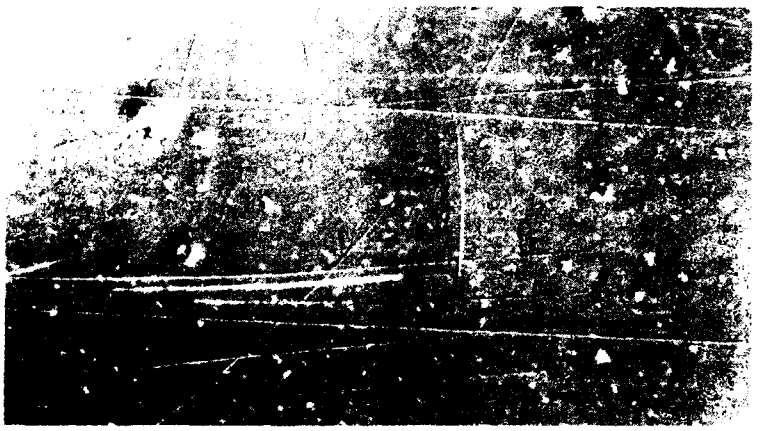


Figure 2. *Steps in planar Gunn diode fabrication:*
(a) n (active) epilayer growth, (b) selective etching of n epilayer, (c) selective refilling of n-layer recesses with n+ (contact) epilayer, and (d) device isolation.

(a)



(b)



(c)

Figure 3. Examples of Fe-doped InP from different sources, etched 3 minutes in $HCl:H_3PO_4$ 1:9: (a) Crysta-Comm material polished in-house by E. R. Schumacher, (b) ICI Americas material polished by ICI, and (c) Sumitomo Electric material polished by Sumitomo. All photos 50X.

precleaning prior to introduction into the growth reactor, selective etching for pattern definition, and ambient conditions once in the growth chamber. Common surface treatment techniques, thought to be standard for other processing, were often found to be too harsh for this device process. Handling and cleaning procedures unique to this device were developed. Such improved techniques have recently found application in new and novel devices currently being fabricated in NOSC's Material and Device Technology Branch (Code 561).

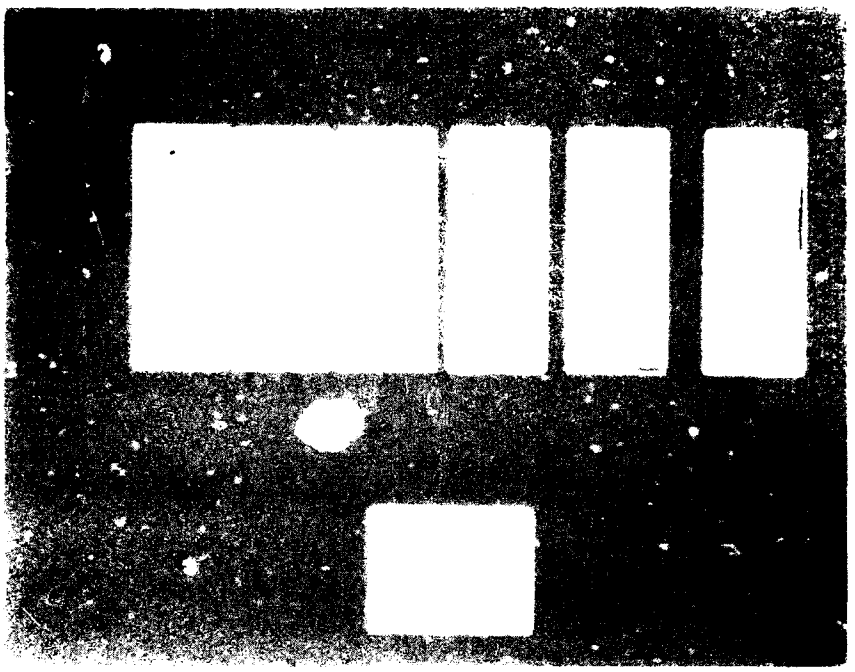
The selective etching process uncovered two potential stumbling blocks. When the first epilayer is selectively removed (exposing the underlying semi-insulating substrate), the exposed surface should be smooth and relatively free of defects for it is on this surface that the second epilayer regrowth will take place. Figure 4 shows examples of a good wafer and a poorly etched wafer. The second epitaxial layer can be expected to nucleate and grow much more nonuniformly in the latter case.

The other stumbling block occurred when masked wafers were sent to Varian Associates for regrowth. Standard procedure was to saturate the indium source with phosphorus trichloride prior to epilayer formation. It was during this time that the pattern was severely etched (figure 5a), resulting in an undercutting of the SiO_2 masking layer to such an extent that no active InP layer remained. As seen in the right-hand side of the photo, the second epilayer was able to grow and actually bury the unsupported oxide "mask" within it. Taking this into account, Varian Associates was able to alter its VPE process, and subsequently provided NOSC with the layer shown in figure 5b.

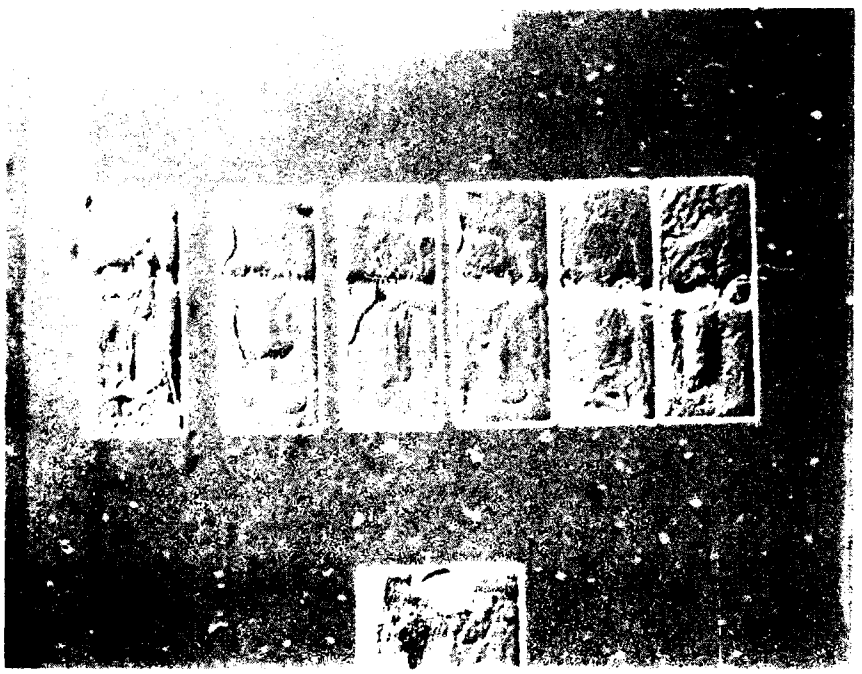
The most severe problem occurred when the in-house MOCVD reactor became contaminated due to failure of the hydrogen purifier to produce dry H_2. Before the problem was discovered, several epilayers were processed for diode use. Figure 6 is an example of growth during this time. Figure 7, a resistance plot of this wafer (M01017/M01052), illustrates the nonuniformity of the layer, not only in surface morphology, but in electrical characteristics as well. (The more uniform the epilayers are, the smaller the spread in resistance measurements.) Figure 8 shows a second growth difficulty. In a few instances, the regrowth epilayer failed to completely fill in the recess area, resulting in a discontinuity between the n^+ contact region and the n active region. The reason for the noncontinuous epilayer growth is not known at this time, although wet H_2 is again suspected.

DEVICE FABRICATION

After the second and final epilayer growth, the SiO_2 masking layer was stripped and the contact resistance of the Gunn device was determined using alloyed gold/germanium contact metal and the transmission line method (TLM) (Look, 1987) of measuring resistance, outlined in figure 9. The objective was to distinguish those structures with low contact resistance (R_C), necessary to permit Gunn oscillation, from others showing too high a resistance. (High contact resistance was also encountered by Varian Associates when they pursued similar work [Cowley, 1984].) There are a number of factors contributing to the resistance value, such as quality of the n/n^+ interface, the carrier concentration of the epilayers, overall layer thickness, and the contact metal/semiconductor interface. Table 1 summarizes the results of the epilayers used on this project.

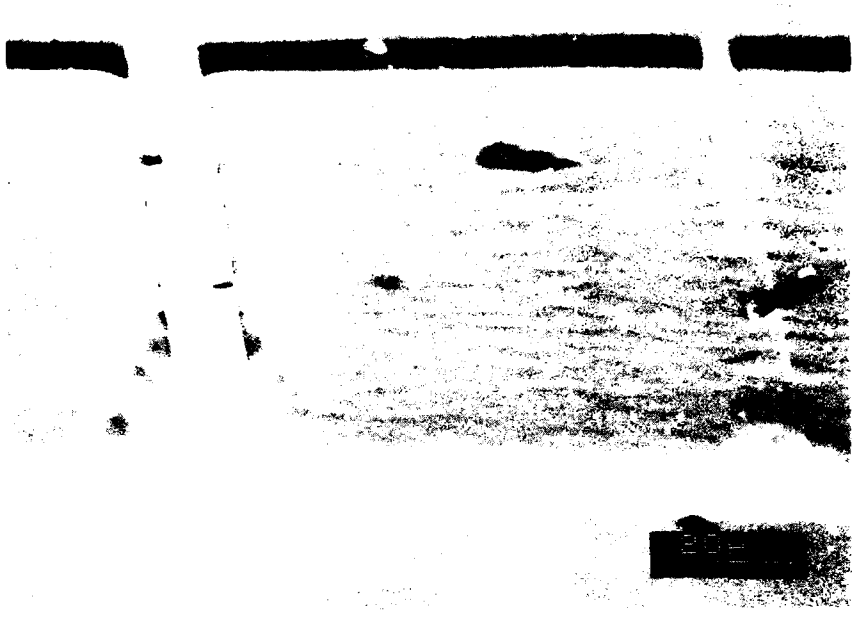


(a)



(b)

Figure 4. Examples of first (undoped) epilayer selectively etched to semi-insulating substrate, prior to regrowth: (a) wafer #M0450, 100×, and (b) wafer #M01016, 100×. The epilayer is removed inside the rectangles.



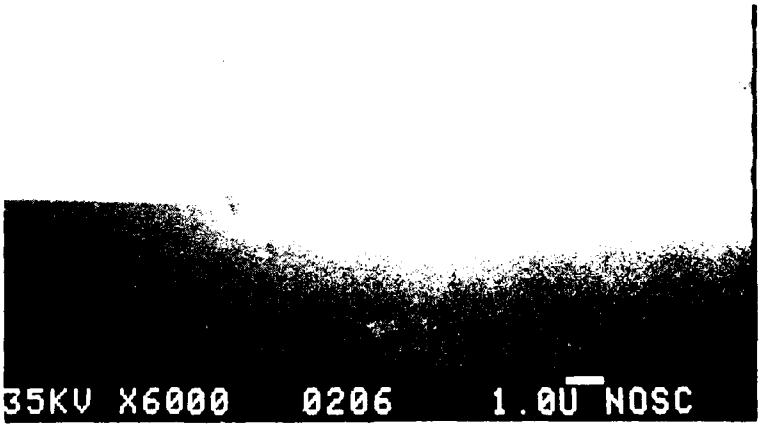
(a)

(b)

Figure 5. (a) Varian wafer #157-2/160-3. Note oxide mask partially covered by second epilayer growth on the right. (b) Varian wafer #157-3/ 160-6 showing minimal undercut of oxide after regrowth.

(a)

(b)



(c)

Figure 6. Wafer #M01017: (a) Before regrowth, layer inside rectangles has been removed, 200×. (b) After regrowth, note texture difference inside and outside of rectangles. (c) SEM photo of regrowth.

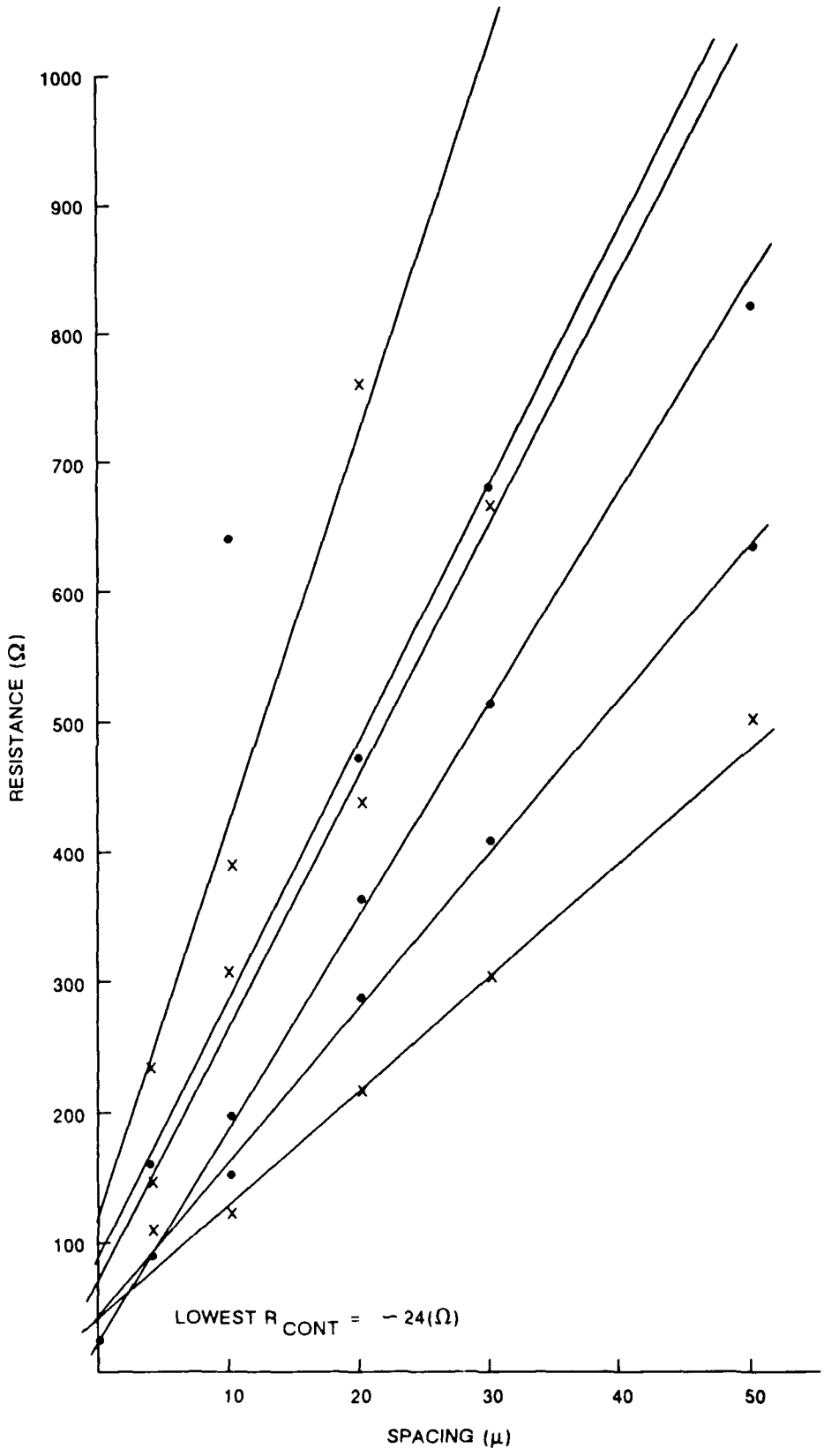
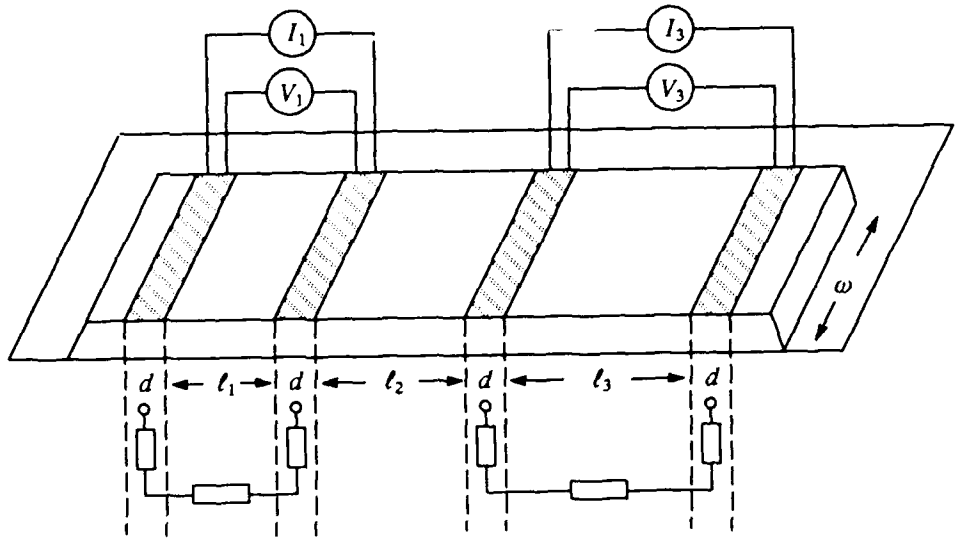


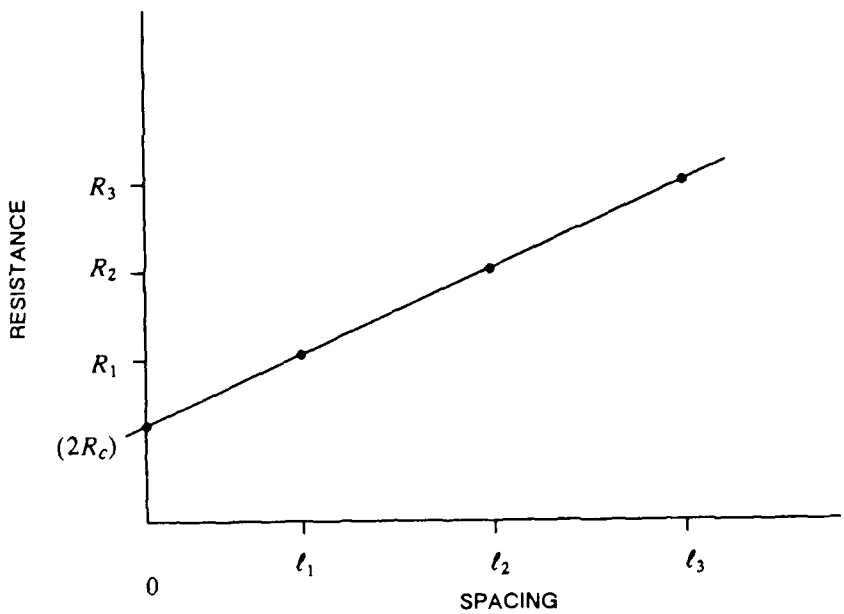
Figure 7. Resistance versus contact spacing, wafer #MO1017/1052.

Figure 8. Wafer #MO1015. Note trench where no regrowth occurred.



$$R_1 = R_c + \frac{R_s \ell_1}{\omega} + R_c \qquad R_c + \frac{R_s \ell_3}{\omega} + R_c = R_3$$

(a)



(b)

Figure 9. (a) Transmission line method (TLM) test pattern. (b) Plot of information collected using TLM pattern.

Table 1. Epilayers and their characteristics used for Gunn diode fabrication.

Substrate	First Epilayer Number	First Epilayer Thickness (μm)	First Epilayer Carrier Concentration (cm ^{3})	Second Epilayer Number	Contact Resistance (Ω)	Test
	446	0.6	7×10^{15}	894		
	450	0.4	9×10^{15}	895		
	450	0.4	9×10^{15}	908/909		
	451	0.5	1.5×10^{16}	919	10	*
	472	0.72	3×10^{16}	920	3	**
	474	0.74	8×10^{15}	896		
2595	904-D2	0.71	5×10^{15}	904/942	-28	
2595	904-D3	0.71	5×10^{15}	944	6	*
2595	905-D2	0.81	5×10^{15}	943	-4	
2595	905-D3	0.81	5×10^{15}	946	7	
	103-5A			941		
	103-5B			945	25	
2682-4B	1015	0.87		1057		
2682-4C	1016	0.55		1060	31	
30-013-1B	1017	0.7	5.5×10^{15}	1052	24	
30-013-1C	1019	1.1		1058	17	*
3140	154-7A	0.64	10^{16}	1056	-4	**
3140	154-7B	0.64	10^{16}	1059	18	
30-013-1	154-8	0.54	10^{16}			
ICI63-2	3-6PM			3-12AM1		
ICI63-3	3-9AM2			3-12AM2		
ICI63-4	3-6AM			3-12PM2		
396-15-A	3-6AM			3-16AM		
396-15-B	3-9AM1			3-12PM2		
396-15-C	3-9AM1			3-12AM1		
396-15-D	3-6PM			3-12AM2		
2682-4D	1054	0.87	4.7×10^{15}	3-12PM1		
2595	705	0.62	3.8×10^{16}			
2595	707	0.66	2.5×10^{16}			
	157-2	0.7	10^{16}	160-3	1	*
	157-3	0.55	10^{16}	160-6	20	*
	157-7	0.55	10^{16}	160-7	4	*

*Tested, but showed no signs of oscillation.
**Tested, oscillated!

The most promising devices (as noted in table 1) were then selected for further processing. This included wafer thinning, gold-plated beam lead formation, and separation of the individual diodes. These topics will be addressed in the following sections.

Wafer Thinning

It was necessary to thin the substrates from 0.020 inch to 0.004 inch to allow for possible heat sinking. The diode fabrication process required that further photolithography be performed after substrate thinning. Hence, the wafers needed to be relatively flat and uniform (suitable for use in a mask aligner) after thinning. Chemical thinning agents were experimented with, but none gave a suitably smooth and flat finished surface. It was, therefore, necessary to chemo-mechanically thin and polish the substrates versus thinning by chemical etching alone.

The nature of the thinning process used required that the blocking side of the wafers be relatively flat. Therefore, wafer thinning and polishing on the backside were accomplished prior to beam lead formation on the frontside. Because of the expense of thinning wafers and their extreme fragility afterwards, all preliminary gold-plating and etching work was done on bulk InP that was 0.020 inch thick.

Gold-Plated Beam Lead Formation

For the diodes to be tested at millimeter-wave frequencies, they had to be attached to hybrid circuits. Wirebonding was ruled out because of the inductance associated with the wire loops. Flat soldered leads were used instead.

The first diodes were attached with gold ribbon leads. Due to the small size of the chip and the active diode region (300 by 250 μm and 3 to 4 μm respectively), hand-soldering the lead to the chip, without damaging the device, was very difficult. Leads were successfully attached to a small group of devices, which were then soldered into the test circuitry. The yield was low and only one device from this first group showed signs of oscillation.

Gold-plated beam leads (see figure 10), produced by photolithography on the whole wafer, were preferred. Not only were the device and lead dimensions more suitable for lithography, but dozens of firmly attached identical leads could be produced at one time. The desire to goldplate onto patterned semiconductor material led to the exploration of several alternative approaches.

Both selective plating and blanket plating followed by selective etching were investigated. Although selective plating appeared simpler, there were two drawbacks. First, the masking resist was not designed for use in such a harsh environment (gold cyanide, heated to 70°C). The resist film reticulated when left in solution for extended periods. Second, not only did the plated gold film mushroom over the top of the resist as anticipated, but the weakened resist film permitted some plating to occur beneath it as well, shorting devices by bridging the contact pads together. Selective etching produced more satisfactory results, despite its drawbacks of poor lithographic image due to the graininess of the plated gold film and difficulty in realigning to features beneath a thick-plated film.

To circumvent the above mentioned problems, different masking layers were tried. Dupont Pyralin PI2570 polyimide, noted for its good adhesion and chemical

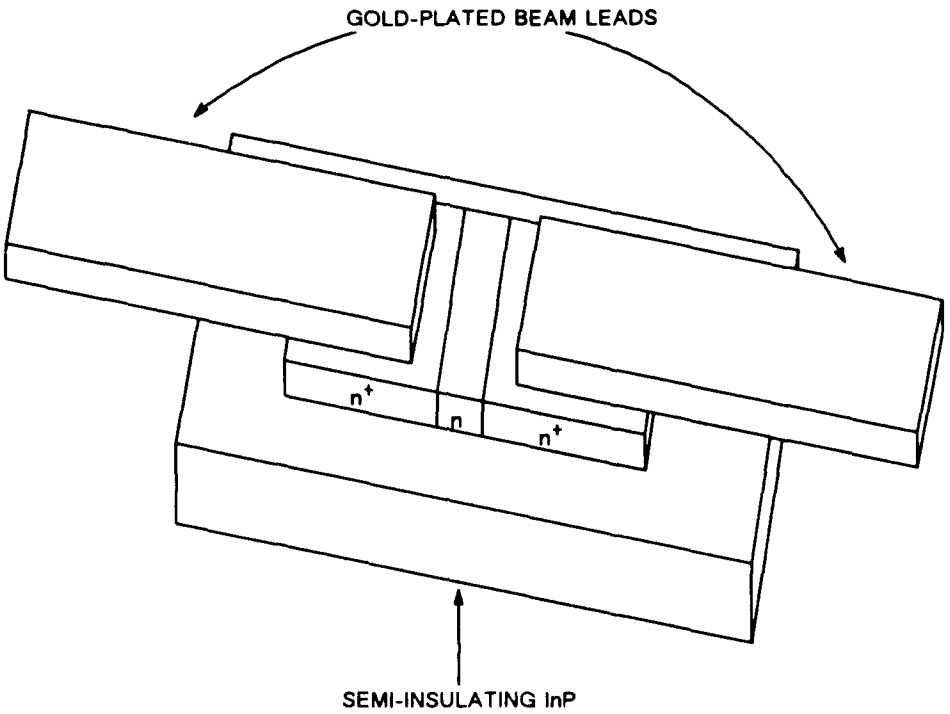


Figure 10. Surface-oriented planar Gunn diode with gold-plated beam leads.

resistance, was not suitable due to the difficulty in removing it for rework and its short shelf life. AZ 4330 photoresist, while providing thick transparent films suitable for plating, did not exhibit adequate chemical resistance. Shipley 1450J photoresist, spun at 4000 r/min, was very easy to process and reasonably resistant to the plating and etching solutions.

Two noteworthy phenomena were observed while goldplating the thinned wafers. Using thick (0.020 inch) wafers, gold was electroplated only in the exposed conductive regions of the front surface. Using thin (0.004 inch) wafers, goldplating also occurred on the sides and back surface of the semi-insulating InP. It is interesting to note that the gold deposits on the back often originated in the thinning sleeks and then spread across the wafer. Also, a faint image of the plated front surface pattern was apparent on the back surface of the thinned wafers. Neither of these phenomena occurred on the thicker wafers.

Die Separation

Originally, the finished diodes were to be individually separated by selectively etching through the substrate from the backside of the wafer. Although many wet etchants were investigated, from concentrated hydrochloric acid to various concentrations of bromine/methanol, they all exhibited severe undercutting of the etch mask. Ferric chloride, a known photochemical etchant for InP (Lubzens, March 1977), was found to be ineffective on semi-insulating material.

Because no suitable chemical etchant was found, the individual beam-leaded diodes were manually diced out. Due to their small size (300 by 250 μm), they were

diced individually under a microscope. At this time, differences in hardness (or brittleness) of the starting bulk material became evident. Some substrates cleaved readily along the desired lines, while others fractured with difficulty and often not at right angles. Figure 11 gives two examples of the finished diodes.

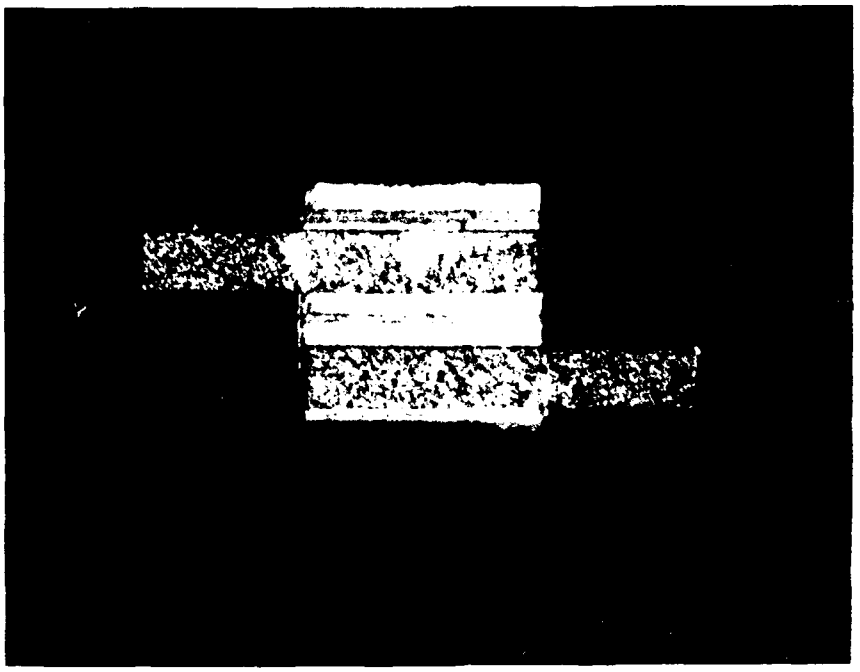
In some instances, the gold-plating on the backside of the wafer remained intact. It was to be utilized for alternative heat-sinking later in the testing. The plated gold film, however, contributed to the difficulty of die separation since it did not necessarily fracture along the same lines as the InP substrate. Those diodes that remained intact at this point were ready for diode testing.

DIODE TESTING

Figure 12 shows the 0.5- by 0.5-inch circuit used for diode testing. The dielectric used was 0.005-inch Rodgers 6010.5 (dielectric constant = 10.5). The upper copper surface was pre-etched to about 0.004 inch to allow 1-mil definition (with little undercutting). Due to the dc block/transformer, a 50-ohm load at the coaxial output should transform to about 5 ohms at the diode. The tuning stub, somewhat longer than 1/4 wavelength, should behave as an inductive reactance at the oscillation frequency, offsetting the diode capacitance. To oscillate, the diode's negative resistance must adjust itself to equal the total circuit positive resistance and the total series reactance must equal zero. In actuality, this happens when the RF voltage swing across the active part of the device changes on both sides of the dc bias point to compensate for the circuit.

Since no heat sink was used for the beam-leaded diodes, the dc power was pulsed, generally less than 0.5 μs. Dozens of diodes from eight different runs were tested. The one run which provided many active devices was from an undoped epilayer grown by Varian Associates with the n^+ contact epilayer regrown in the recesses using NOSC's MOCVD reactor. The diodes showing oscillation were fabricated with sloped n/n^+ interfaces. The companion wafer (the same epilayer runs but with vertical n/n^+ interfaces) did not survive to the beam lead stage. This was unfortunate since the resistance measurements looked promising and a direct comparison of geometry was desired.

Results on the one good wafer included pulsed power in the 4-mW range and oscillation frequencies in the 20- to 40-GHz region. Attempts at heat-sinking, by bonding the diode to the fixture surface through a hole in the substrate with conductive epoxy, were unsuccessful.



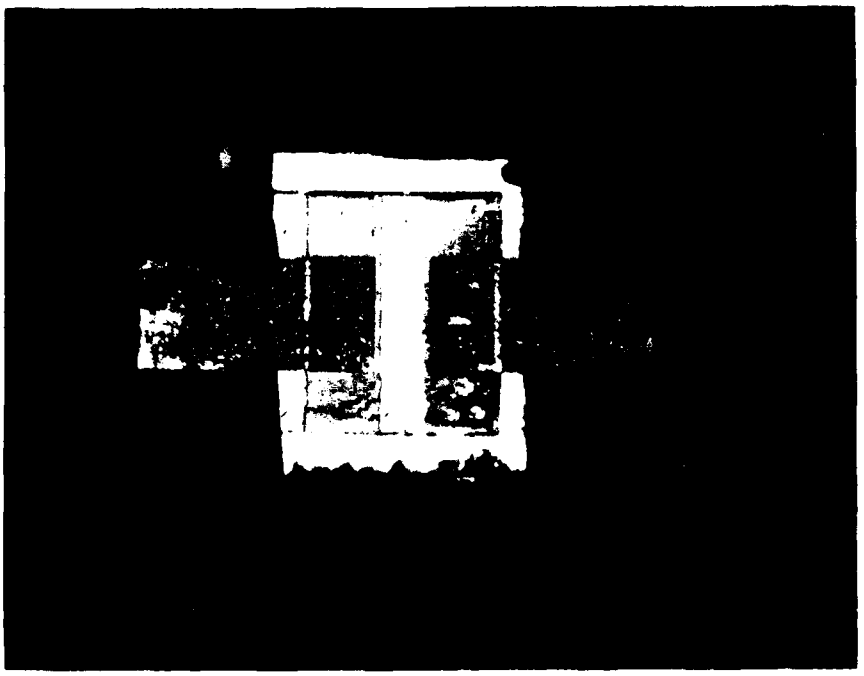


Figure 11. Two examples of finished (beam-leaded) devices.

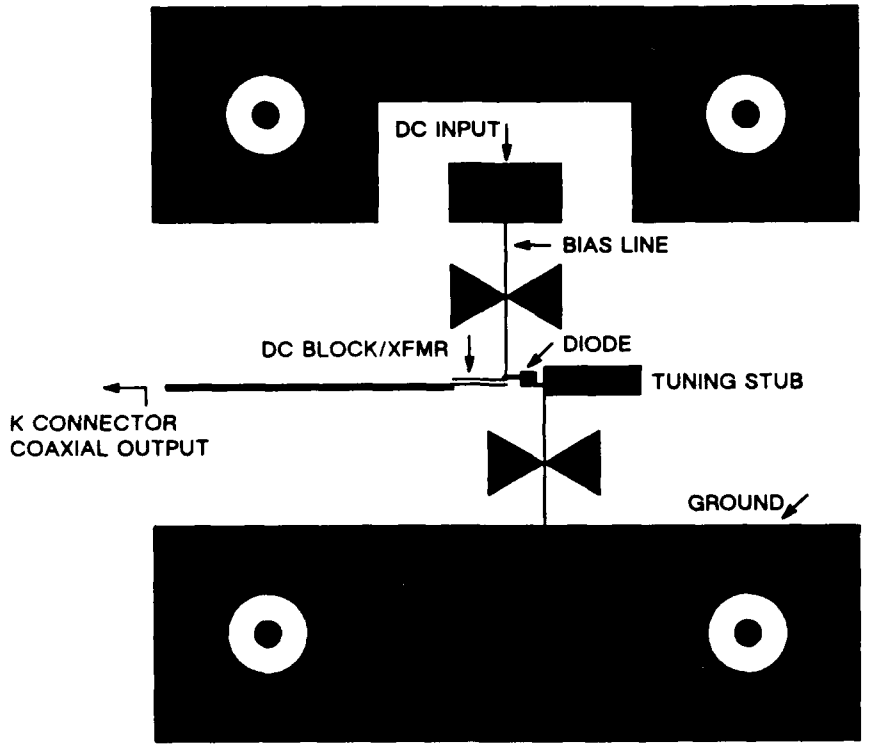


Figure 12. RF circuit used for testing beam-leaded InP Gunn diodes.

SUMMARY AND FUTURE CONSIDERATIONS

SUMMARY

A Gunn diode that exhibited oscillations within the 20- to 40-GHz-frequency range was successfully fabricated using epitaxially grown layers. The concept of selectively removing portions of one epilayer and then refilling the recesses with a second epilayer was demonstrated. The working structure showed low resistance across the n/n^+ interface, as expected.

All of the processing techniques developed for the InP Gunn diode work have been incorporated into current work in Code 561. The vertical sidewall etching is being used to fabricate self-aligned junction field-effect transistors (JFETs). Regrowth in selected recesses is being utilized to fabricate p-i-n photodiodes as part of an InP integrated circuit. Thinned InP wafers are used when testing microwave devices such as power FETs, amplifiers, and photoconductive switches. Plated beam leads are used to attach discrete switches to test circuitry.

In addition, the successful Gunn diodes fabricated and tested during this project have renewed Varian Associates' interest in surface-oriented planar Gunn diodes. NOSC is currently collaborating with Varian Associates in this effort. Epilayers are being provided by Varian Associates, and device-fabrication and testing are being done at NOSC.

FUTURE CONSIDERATIONS

Areas of further interest stimulated by this project include the following four topics. First, the effect of backside thinning on frontside device performance should be investigated. Several interesting effects became evident when the plating process on thin wafers was compared with the process on thick wafers. The thin wafers plated as though they were conducting, instead of semi-insulating, substrates. Also, images of front surface features appeared on the back surface of the thinned wafers during plating. Neither of these two effects were seen when plating the thicker wafers.

Second, the technique of recessed regrowth in selective areas is extremely useful when fabricating planar (versus mesa) integrated circuits. But more work is needed in this area. The Gunn diode yield was much less than 100 percent and more work is required to improve this yield. Increased understanding is needed in the areas of growth nucleation (or lack of it), effects of surface preparation, and effect of crystal orientation on regrowth.

Third, the vertical etch process may have introduced crystal surfaces that were not only resistant to etching but resistant to regrowth nucleation as well. This, in turn, may have contributed to the low yield of suitable epilayers for this work. A more thorough study is needed to determine why certain epilayers failed to support a regrowth layer.

Finally, a topic of special interest is the task of separating individual devices from the process wafer by backside etching, as opposed to scribing or dicing. Attempts were made at wet-chemical etching but the etchants investigated were either ineffective on semi-insulating material or undercut so severely that the masking layer was completely removed. For technology transfer, an automated (versus the labor-intensive manual dicing) procedure is necessary.

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[1]NOSC Technical Notes (TNs) are working documents and do not represent an official policy statement of the Naval Ocean Systems Center. For further information, contact the author.

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13 ABSTRACT (Maximum 200 words)

An indium phosphide (InP) planar Gunn diode showing oscillations in the 20- to 40-GHz-frequency range was successfully fabricated and tested using epitaxially grown layers. Also demonstrated was the concept of selectively removing portions of one epilayer and refilling the recesses with a second epilayer. The working structure showed low resistance across the n/n^+ interface.

Processing techniques developed during the InP planar Gunn diode work are now incorporated into current work at NOSC. Also, successes in these experiments resulted in renewed interests in surface-oriented planar Gunn diodes.

14 SUBJECT TERMS

indium phosphide (InP), vapor phase epitaxy (VPE), planar Gunn diode, metalorganic chemical vapor deposition (MOCVD), monolithic circuits, epilayer growth, substrates

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